

# TG7221B-T5JE0

High Performance Low Power Bluetooth 5.2 SoC

Preliminary Datasheet

## General Descriptions

TG7221B-T5JE0 is a highly integrated SoC with Bluetooth 5.2 dual mode and high performance audio Codec. It also integrates 32 bit MCU and 192MHz Risc-V MCU to support various software features and product customization. TG7221B-T5JE0 has been designed on highest level of integration to extremely reduce the number of external component. It is manufactured with advanced 55nm CMOS low leakage process which offers highest integration, lowest power consumption, lowest leakage current and reduced BOM cost.

## Key Features

- Dual CPU Architecture
  - 32bit-Risc Core for link management
    - 96kB code ROM and 512bit EFUSE
    - 8kB patch RAM and 20kB data RAM
    - 4kB RAMs can be set to retention mode
  - Risc-V Core for application
    - Data RAM 56kB+Cache 16kB
    - Up to 192MHz with float point unit
- Audio Codec
  - Stereo 24-bit DAC, SNR $\geq$ 109dB
  - Mono 16-bit ADC, SNR $\geq$ 98dB
  - Supports one PDM digital MIC inputs
  - Sampling rates of 8KHz/11.025KHz/16KHz/22.05KHz/24KHz/32KHz/44.1KHz/48KHz are supported
  - Analog MIC amplifier, build-in MIC bias generator
  - Two channels Stereo analog MUX
  - Supports cap-less, single-ended, and differential mode at the DAC path
  - Supports 16ohm and 32ohm Speaker loading
- Bluetooth 5.2 transceiver
  - +12 dBm TX power in 1dB/steps@BLE
  - +7 dBm TX power in 1dB/steps@EDR
  - -99 dBm RX sensitivity @ BLE 1 Mbps
  - -95 dBm RX sensitivity @ EDR 2 Mbps
  - Fast AGC for enhanced dynamic range
- PMU
  - Built-in LDO and DC-DC for the core, I/O, Bluetooth and flash
  - Built-in charger for battery
  - 1.6 uA current consumption in the soft-off mode
  - VBAT is 2.2V to 4.5V;
- VDDIO is 2.2V to 3.6V;
- Audio Processing
  - SBC, AAC, LC3 Audio decodes supported for BT audio
  - mSBC voice codec supported for BT voice
  - Supports MP3, WMA, FLAC, AAC, WAV, OPUS audio decoding
  - Packet Loss Concealment (PLC) for voice processing
  - Acoustic echo cancellation/suppression (AEC,AES)
  - Single MIC Environmental Noise Cancellation (ENC)
  - Multi-band DRC limiter and Noise gate
  - Multi-band EQ and Bass enhancement
- Peripherals
  - Up to 38 GPIOs with functions fully multiplexed
  - 8-channel 10-bit ADC
  - Built-in Low power Touch Key
  - Built-in Low power enter ear detect
  - Built-in IR circuit
  - Two-wire Master (I2C compatible), up to 600kbps;
  - Two UART(RTS/CTS) with HCI-H5 protocol, up to 3.25Mbps;
  - SPI Master support
  - Three QSPI support
  - 8x PWM support
  - USB2.0 full speed, support host/slave mode
  - SD Card Host Controller support
  - I2S master/slave support
- RF
  - Supports for DCXO with internal oscillator circuit

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## Revision History

Version	Date	Owner	Note
0.1	12/09/2021	ZG	Initial version
0.2	13/10/2023	ZG	Initial version

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## Contents

General Descriptions.....	1
<b>Key Features</b> .....	<b>1</b>
Revision History.....	2
Contents.....	3
List of Figures.....	4
List of Tables.....	5
1 Block Diagram.....	6
2 Pinout Information.....	7
3 Specifications.....	10
3.1 Recommended Operating Conditions.....	10
3.2 Power Consumption.....	10
3.3 Radio.....	11
3.4 24 MHz Crystal Oscillator.....	14
3.5 LDO Characteristics.....	14
3.6 Reset Characteristics.....	14
3.7 DAC Characteristics.....	15
3.8 ADC Characteristics.....	15
4 Application Schematic.....	16
5 Package Information.....	17

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## List of Figures

Figure 1- 1	Block diagram .....	6
Figure 2- 1	Pinout top view (TSSOP24 package).....	7
Figure 5- 1	TSSOP24 package dimensions.....	17

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## List of Tables

Table 2- 1	Pinout Information of TSSOP24	8
Table 2- 2	GPIO Multiplexing	9
Table 3- 1	Recommended Operation Condition	10
Table 3- 2	Power Consumption Characteristics	10
Table 3- 3	Transmitter Specification	11
Table 3- 4	Receiver Specification	12
Table 3- 5	24 MHz Crystal Oscillator Characteristic	14
Table 3- 6	LDO Specification	14
Table 3- 7	Reset Characteristics	14
Table 3- 8	Audio DAC Characteristics	15
Table 3- 9	Audio ADC Characteristics	15

# 1 Block Diagram

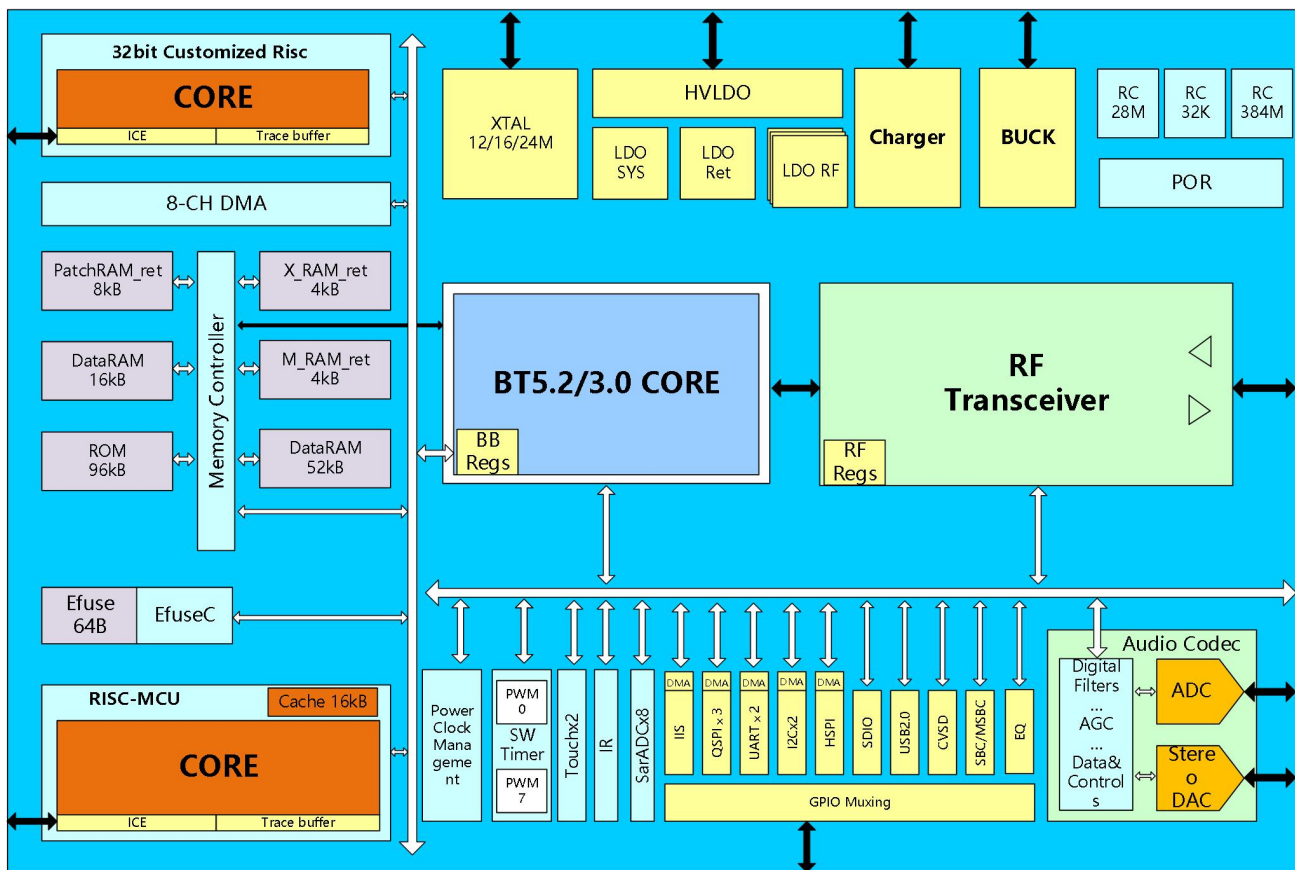


Figure 1-1 Block diagram

## 2 Pinout Information

<b>RF</b>	<b>1</b>	<b>TG7221B-T5JE0</b> <b>TSSOP24</b>	<b>24</b>	<b>GPIO34/ TOUCH2</b>
<b>GND</b>	<b>2</b>		<b>23</b>	<b>GPIO33/ TOUCH1</b>
<b>XTALIN</b>	<b>3</b>		<b>22</b>	<b>GPIO25</b>
<b>XTALOUT</b>	<b>4</b>		<b>21</b>	<b>GPIO24/ADC</b>
<b>VBAT</b>	<b>5</b>		<b>20</b>	<b>GPIO23/ADC</b>
<b>GPIO2</b>	<b>6</b>		<b>19</b>	<b>GPIO13/ TOUCH2</b>
<b>GPIO1</b>	<b>7</b>		<b>18</b>	<b>GPIO12/ TOUCH1</b>
<b>GPIO0</b>	<b>8</b>		<b>17</b>	<b>GPIO11</b>
<b>GPIO4/IR</b>	<b>9</b>		<b>16</b>	<b>ICE</b>
<b>GPIO5/ADC</b>	<b>10</b>		<b>15</b>	<b>GPIO10/ TOUCH2</b>
<b>GPIO6/ADC</b>	<b>11</b>		<b>14</b>	<b>GPIO9/ TOUCH1</b>
<b>GPIO7/ADC</b>	<b>12</b>		<b>13</b>	<b>GPIO8/ADC</b>

Figure 2- 1 Pinout top view (TSSOP24 package)

Abbreviations:

PWR: Power pin

AIO: Analog IO pin

DIO: Digital IO pin

RF: RF IO pin

Table 2- 1 Pinout Information of TSSOP24

TSSOP24	Pin Name	Type	Function Description
1	RF	RF_Port	ANT port
2	GND	GND	GND port
3	XTALIN	Ana_I	24M Crystal oscillator input
4	XTALOUT	Ana_O	24M Crystal oscillator output
5	VBAT	Power_I	Battery input
6	GPIO2	Dig_IO	pls check "sheet: GPIO_Muxing";
7	GPIO1	Dig_IO	pls check "sheet: GPIO_Muxing";
8	GPIO0	Dig_IO	pls check "sheet: GPIO_Muxing";
9	GPIO4/IR	Dig_IO/Ana	pls check "sheet: GPIO_Muxing"; Nec in IR out
10	GPIO5/ADC	Dig_IO/Ana_O	pls check "sheet: GPIO_Muxing"; Measure Sar ADC
11	GPIO6/ADC	Dig_IO/Ana_O	pls check "sheet: GPIO_Muxing"; Measure Sar ADC
12	GPIO7/ADC	Dig_IO/Ana_O	pls check "sheet: GPIO_Muxing"; Measure Sar ADC
13	GPIO8/ADC	Dig_IO/Ana_O	pls check "sheet: GPIO_Muxing"; Measure Sar ADC
14	GPIO9/TOUCH1	Dig_IO/Ana_O	pls check "sheet: GPIO_Muxing"; Touch pad 1
15	GPIO10/TOUCH2	Dig_IO/Ana_O	pls check "sheet: GPIO_Muxing"; Touch pad 2
16	ICE	Dig_IO	pls check "sheet: GPIO_Muxing"
17	GPIO11	Dig_IO	pls check "sheet: GPIO_Muxing";
18	GPIO12/TOUCH1	Dig_IO/Ana_O	pls check "sheet: GPIO_Muxing"; Touch pad 1
19	GPIO13/TOUCH2	Dig_IO/Ana_O	pls check "sheet: GPIO_Muxing"; Touch pad 2
20	GPIO23/ADC	Dig_IO/Ana_O	pls check "sheet: GPIO_Muxing"; Measure Sar ADC
21	GPIO24/ADC	Dig_IO/Ana_O	pls check "sheet: GPIO_Muxing"; Measure Sar ADC
22	GPIO25	Dig_IO	pls check "sheet: GPIO_Muxing";
23	GPIO33/TOUCH1	Dig_IO/Ana_O	pls check "sheet: GPIO_Muxing"; Touch pad 1
24	GPIO34/TOUCH2	Dig_IO/Ana_O	pls check "sheet: GPIO_Muxing"; Touch pad 2



Table 2- 2 GPIO Multiplexing

Pin Name	boot function	function-analog
GPIO[0]		xtal32k_in
GPIO[1]		xtal32k_out
GPIO[2]		
GPIO[3]		
GPIO[4]		Charge uart
GPIO[5]		saradc [0]
GPIO[6]		saradc [1]
GPIO[7]		saradc [2]
GPIO[8]		saradc [3]
GPIO[9]	EXEN	linein_r/Touch1_pad_c
GPIO[10]		linein_l/Touch2_pad_c
GPIO[11]	IO_RST	
GPIO[12]		Touch1_pad_b
GPIO[13]		Touch2_pad_b
GPIO[14]		
GPIO[15]		
GPIO[16]		
GPIO[17]		
GPIO[18]		
GPIO[19]		
GPIO[20]		
GPIO[21]		
GPIO[22]		
GPIO[23]		saradc [4]
GPIO[24]		saradc [5]
GPIO[25]		
GPIO[26]		
GPIO[27]		
GPIO[28]		
GPIO[29]		
GPIO[30]		

GPIO[31]		
GPIO[32]		
GPIO[33]	IO_RST	saradc [6]/Touch1_pad_a
GPIO[34]		saradc [7]/Touch2_pad_a
GPIO[35]	ICE/IO_RST	
GPIO[36]		
GPIO[37]		

Note: PWM, UART, SPI and other digital peripherals can be flexibly configured to any GPIO port

## 3 Specifications

### 3.1 Recommended Operating Conditions

Table 3-1 Recommended Operation Condition

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage for pin VBAT	$V_{BAT}$		2.2	3.3	5.5	V
Supply voltage for pin VDCDC	$V_{DCDC}$		1.25	3.3	5.5	V
Supply voltage for pin VIO	$V_{IO}$		2.2	3.3	3.6	V
Supply voltage for Charger	$V_{LDO\_IN}$		4.5		5.5	V
Charge voltage	$V_{Charge}$		4.5	5	5.4	V
Charge Current	$I_{Charge}$		20	40	170	mA
Trickle Charge Current	$I_{Trickle}$		2	16	68	mA
Ambient temperature	$T_A$		-40		110	°C

### 3.2 Power Consumption

Table 3-2 Power Consumption Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sleep						
Current through pin VBAT	$I_{VBAT\_SLEEP}$	$V_{BAT} = 3.3V$		1.3		μA
	$I_{VBAT\_SLEEP\_RET}$			2.0		μA
Current through pin VDCDC	$I_{VDCDC\_SLEEP}$	$V_{DCDC} = 1.2V$		20.0		nA
RX mode 1 Mbps BLE @ -99 dBm sensitivity						
Current through pin VBAT	$I_{VBAT\_RX}$	$V_{BAT} = 3.3V$		0.48		mA
Current through pin VLDO	$I_{VLDO\_RX}$	$V_{DLDO} = 1.2V$	9.5	10.5	12.5	mA

Current through pin VDCDC	$I_{VDCDC\_RX}$	$V_{LDO} = 1.2V$	5.8	6.3	7.2	mA
RX mode 1 Mbps BLE @ -97 dBm sensitivity						
Current through pin VBAT	$I_{VBAT\_RX}$	$V_{BAT} = 3.3V$		0.48		mA
Current through pin VLDO	$I_{VLDO\_RX}$	$V_{DLDO} = 1.2V$	8	9	11	mA
Current through pin VDCDC	$I_{VDCDC\_RX}$	$V_{LDO} = 1.2V$	5.6	5.9	7	mA
TX mode 0 dBm						
Current through pin VBAT	$I_{VBAT\_TX}$	$V_{BAT} = 3.3V$		0.48		mA
Current through pin VLDO	$I_{VLDO\_TX}$	$V_{DCDC} = 1.2V$	15.5	16.0	17.5	mA
Current through pin VDCDC	$I_{VDCDC\_TX}$	$V_{LDO} = 1.2V$	9.2	9.5	10.2	mA

### 3.3 Radio

All parameters are referred to chip port and measured on the condition of  $V_{BAT} = V_{IN} = 3.3V$  if not stated otherwise.

Table 3-3 Transmitter Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	$f_{TX}$		2325		2740	MHz
Output power	$P_{out}$		-20.0		15.0	dBm
Power control step	$P_{step}$	For part-to-part power calibrations	0.5	1.0		dB
2 <sup>nd</sup> harmonic power	$P_{2harm}$	0 dBm		-45.0		dBm
		4 dBm		-40.0		dBm
		12 dBm		-25.5		dBm
3 <sup>rd</sup> harmonic power	$P_{3harm}$	0 dBm				dBm
		4 dBm				dBm
		12 dBm				dBm
4 <sup>th</sup> harmonic power	$P_{4harm}$	0 dBm				dBm
		4 dBm				dBm
		12 dBm				dBm
Spurious emissions (@ 4 dBm)	$P_{spur}$	30 MHz to 1000 MHz		-43.7		dBm
		1 GHz to 12.75 GHz		-31.0		dBm
		47 MHz to 74 MHz		-75		dBm
		87.5 MHz to 108 MHz		-75		dBm
		174 MHz to 230 MHz		-75		dBm
		470 MHz to 862 MHz		-44.0		dBm
<b>BDR DH1</b>						
Average frequency deviation	$\Delta f1_{avg\_BR}$	0 dBm	156	159	162	KHz
		4 dBm	155	159.5	163	KHz
		11 dBm	153	160	169	KHz
Average frequency deviation ratio	$\Delta f2_{avg\_BR} / \Delta f1_{avg\_BR}$	0 dBm	0.9	0.915	0.93	
		4 dBm	0.89	0.91	0.94	
		11 dBm	0.86	0.92	0.99	

Adjacent channel power (2MHz offset)	$P_{adj\_BR}$	0 dBm	-55	-51.3	-50	dBm
		4 dBm	-53	-48.6	-47	dBm
		11 dBm	-42	-39.7	-38	dBm
Alternate adjacent channel power (3MHz offset)	$P_{aadj\_BR}$	0 dBm	-58	-54.3	-53	dBm
		4 dBm	-54	-52	-51	dBm
		11 dBm	-49	-43.2	-41	dBm
<b>EDR 2DH5</b>						
PRF	RF output power		-20	0	8	dBm
PRF1	Adjacent channel power (2MHz offset)@0dBm			-32		dBm
PRF2	Adjacent channel power (3MHz offset)@0dBm			-36.5		dBm
Modulation Accuracy, EVM	RMS DEVM ( $\pi/4$ DQPSK) @0dBm			5		%
	Peak DEVM ( $\pi/4$ DQPSK) @0dBm			14		%
<b>1 Mbps BLE</b>						
Average frequency deviation	$\Delta f_{1\_avg\_1M}$	0 dBm	244	248.6	251	KHz
		4 dBm	242	248.1	253	KHz
		12 dBm	244	249.3	257	KHz
Average frequency deviation ratio	$\frac{\Delta f_{2\_avg\_1M}}{\Delta f_{1\_avg\_1M}}$	0 dBm	0.89	0.914	0.95	
		4 dBm	0.89	0.914	0.97	
		12 dBm	0.83	0.89	0.99	
Adjacent channel power (2 MHz offset)	$P_{adj\_1M}$	0 dBm	-54	-51.4	-47	dBm
		4 dBm	-50	-47.4	-44	dBm
		12 dBm	-42	-37.4	-32	dBm
Alternate adjacent channel power (3 MHz offset)	$P_{aadj\_1M}$	0 dBm	-57	-55.3	-53	dBm
		4 dBm	-53	-51.1	-46	dBm
		12 dBm	-46	-42.2	-39	dBm
<b>2 Mbps BLE</b>						
Average frequency deviation	$\Delta f_{1\_avg\_2M}$	0 dBm	494	497.6	502	KHz
		4 dBm	491	598.6	505	KHz
		12 dBm	470	598.3	518	KHz
Average frequency deviation ratio	$\frac{\Delta f_{2\_avg\_2M}}{\Delta f_{1\_avg\_2M}}$	0 dBm	0.87	0.89	0.9	
		4 dBm	0.86	0.89	0.91	
		12 dBm	0.81	0.86	0.97	
Adjacent channel power (4 MHz offset)	$P_{adj\_2M}$	0 dBm	-59	-56.5	-54	dBm
		4 dBm	-54	-52.3	-47	dBm
		12 dBm	-47	-42.5	-34	dBm
Alternate adjacent channel power (6 MHz offset)	$P_{aadj\_2M}$	0 dBm	-61	-58.9	-55	dBm
		4 dBm	-56	-54.3	-48	dBm
		12 dBm	-49	-44.7	-40	dBm

Table 3- 4 Receiver Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	$f_{RX}$		2325		2740	MHz
Out-of-band blocking	OOB	30 MHz – 2000 MHz	-30			dBm
		2003 – 2399 MHz	-35			dBm
		2484 – 2997 MHz	-35			dBm

		3000 MHz – 12.75 GHz	-30			dBm
<b>Basic Rate</b>						
RX sensitivity	$P_{SENS\_BR}$	0.1 % BER	-97	-95.4	-94	dBm
C/I co-channel	$C/I_{CO\_BR}$	0.1 % BER		7.1	11	dB
C/I 1 MHz adjacent channel	$C/I_{1\_1M}$	0.1 % BER		-9.2	0	dB
C/I 2 MHz adjacent channel	$C/I_{2\_1M}$	0.1 % BER		-38.1	-30	dB
C/I $\geq 3$ MHz adjacent channel	$C/I_{3\_1M}$	0.1 % BER		-44.9	-40	dB
C/I image channel	$C/I_{im\_1M}$	0.1 % BER		-26.0	-9	dB
C/I image channel + 1MHz	$C/I_{im+1\_1M}$	0.1 % BER		-39.5	-20	dB
Maximum input signal level	$P_{IN\_MAX\_1M}$	0.1 % BER		0.0	-20	dBm
<b>EDR 2DH5</b>						
RX sensitivity	$P_{SENS\_BR}$	0.01 % BER	-95	-93.5	-92	dBm
C/I co-channel	$C/I_{CO\_BR}$	0.01 % BER		9	13	dB
C/I 1 MHz adjacent channel	$C/I_{1\_1M}$	0.01 % BER		-9	0	dB
C/I 2 MHz adjacent channel	$C/I_{2\_1M}$	0.01 % BER		-40	-30	dB
C/I $\geq 3$ MHz adjacent channel	$C/I_{3\_1M}$	0.01 % BER		-42	-40	dB
C/I image channel	$C/I_{im\_1M}$	0.01 % BER		-27	-7	dB
C/I image channel + 1MHz	$C/I_{im+1\_1M}$	0.01 % BER		-41	-20	dB
Maximum input signal level	$P_{IN\_MAX\_1M}$	0.01 % BER		-10	-20	dBm
<b>1 Mbps BLE</b>						
RX sensitivity	$P_{SENS\_1M}$	30.8 % PER	-100.5	-99.3	-97	dBm
C/I co-channel	$C/I_{CO\_1M}$	30.8 % PER		3.8	21	dB
C/I 1 MHz adjacent channel	$C/I_{1\_1M}$	30.8 % PER		-23.6	15	dB
C/I 2 MHz adjacent channel	$C/I_{2\_1M}$	30.8 % PER		-26.8	-17	dB
C/I $\geq 3$ MHz adjacent channel	$C/I_{3\_1M}$	30.8 % PER		-37.9	-27	dB
C/I image channel	$C/I_{im\_1M}$	30.8 % PER		-30.5	-9	dB
C/I image channel + 1MHz	$C/I_{im+1\_1M}$	30.8 % PER		-45	-15	dB
Maximum input signal level	$P_{IN\_MAX\_1M}$	30.8 % PER		0.0	-10	dBm
<b>2 Mbps BLE</b>						
RX sensitivity	$P_{SENS\_2M}$	30.8 % PER	-96.5	-96	-95	dBm
C/I co-channel	$C/I_{CO\_2M}$	30.8 % PER		3.2	21	dB
C/I 2 MHz adjacent channel	$C/I_{2\_2M}$	30.8 % PER		3.8	15	dB
C/I 4 MHz adjacent channel	$C/I_{4\_2M}$	30.8 % PER		-35	-17	dB
C/I $\geq 6$ MHz adjacent channel	$C/I_{6\_2M}$	30.8 % PER		-40.5	-27	dB
C/I image channel	$C/I_{im\_2M}$	30.8 % PER		-20.1	-9	dB
C/I image channel + 2MHz	$C/I_{im+2\_2M}$	30.8 % PER		-35	-15	dB
Maximum input signal level	$P_{IN\_MAX\_1M}$	30.8 % PER		0.0	-10	dBm

### 3.4 4 MHz Crystal Oscillator

Table 3- 5 24 MHz Crystal Oscillator Characteristic

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency	$f_{XTAL}$		16	24	32	MHz
Crystal frequency tolerance	$\Delta f_{XTAL}$		-50		50	ppm
Load capacitance	$C_{L,INN}$	Programmable via registers		12	20	pF
Phase noise (referred to 24 MHz)	$PN_{XTAL}$	24 MHz at 100Hz offset		-115		dBc/Hz
		24 MHz at 1KHz offset		-125		dBc/Hz
		24 MHz at 10KHz offset		-135		dBc/Hz
		24 MHz at 100KHz offset		-142		dBc/Hz
		24 MHz at 1MHz offset		-146		dBc/Hz
Duty cycle	$DC_{XTAL}$		40.0	50.0	60.0	%
Startup time	$T_{ST}$	Amplitude settles to $\pm 80\%$ its normal value		1.5		mS

### 3.5 LDO Characteristics

Table 3- 6 LDO Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage range	$V_{IN}$				5.5	MHz
Output voltage	$V_{OUT,SLEEP}$	$I_{LOAD}=20$ mA, when input voltage below 3.3V, output equals input		3.35		V
	$V_{OUT,ACTIVE}$	$I_{LOAD}=100$ $\mu$ A, when input voltage below 3.3V, output equals input		3.35		V
Maximum load current	$I_{LOAD}$	Active mode		40		mA
Output load capacitance	$C_L$		0		1	$\mu$ F
Quiescent current	$I_{Q,SLEEP}$	doze mode		50		nA
	$I_{Q,ACTIVE}$	active mode		50		$\mu$ A

### 3.6 Reset Characteristics

Reset voltage is monitored on pin VBAT\_HIGH.

Table 3- 7 Reset Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset voltage threshold	$V_{POR}$	rising edge	1.60	1.80	2.0	V
	$V_{PDR}$	falling edge	1.50	1.70	1.90	V
POR stretch time	$T_{POR}$			20.00		mS
PDR stretch time	$T_{PDR}$			20		$\mu$ S

### 3.7 DAC Characteristics

Table 3- 8 Audio DAC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			24		Bits
Full Scale Output Signal Level	AVDD=2.5V		1.6		Vrms
Sampling frequency		8		48	kHz
Dynamic Range	A- Weighted , 1kHz, -60dBFS input signal		105		dB
Signal to Noise Ratio	A- Weighted , 1kHz, 0dBFS, input signal		109		dB
Total Harmonic Distortion + Noise	Weighted ,1kHz, -6dBFS, input signal		-91		dB
Channel Separation			119		dB

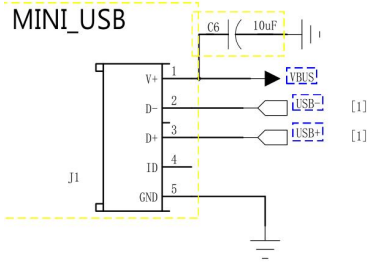
### 3.8 ADC Characteristics

Table 3- 9 Audio ADC Characteristics

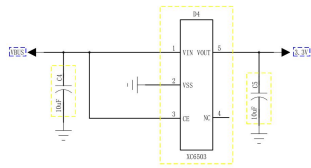
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			16		Bits
Full Scale input Signal Level	AVDD=2.5V Mic gain=0		1.6		Vrms
Sampling frequency		8		48	kHz
PGA Gain Range	1.5dB/step	0		46.5	dB
Input Resistance		20			kΩ
Dynamic Range	A-Weighted 1kHz input signal		98		dB
Signal to Noise Ratio	A-Weighted, 1kHz input signal		98		dB
Total Harmonic Distortion + Noise	Mic gain=0, Generator Level=2vrms, -1.2dbfs,1kHz input signal		-91		dB

# 4 Application Schematic

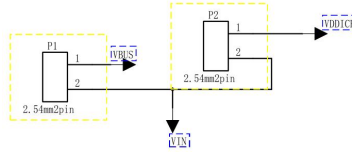
## USB



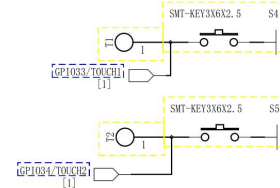
## POWER



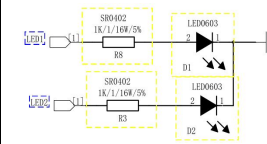
## SEL 供电选择, 方便测试测各模块电流



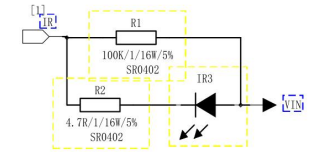
## TOUCH



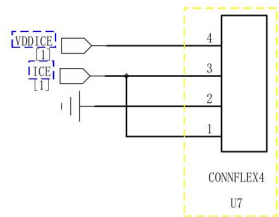
## LED



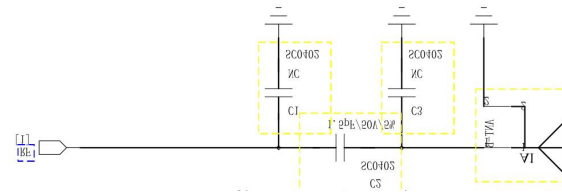
## IR



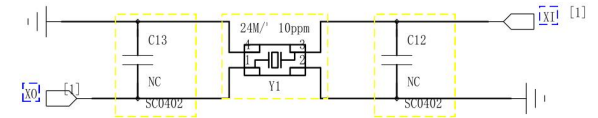
## ICE



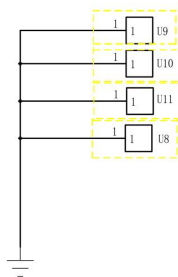
## RF 预留π型匹配网络, 具体以实测为准



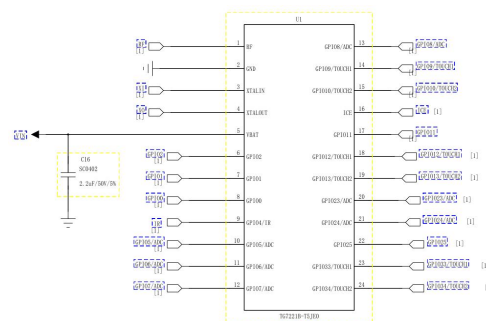
## XTAL



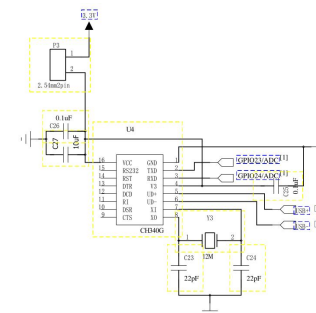
## LOGO



## MCU

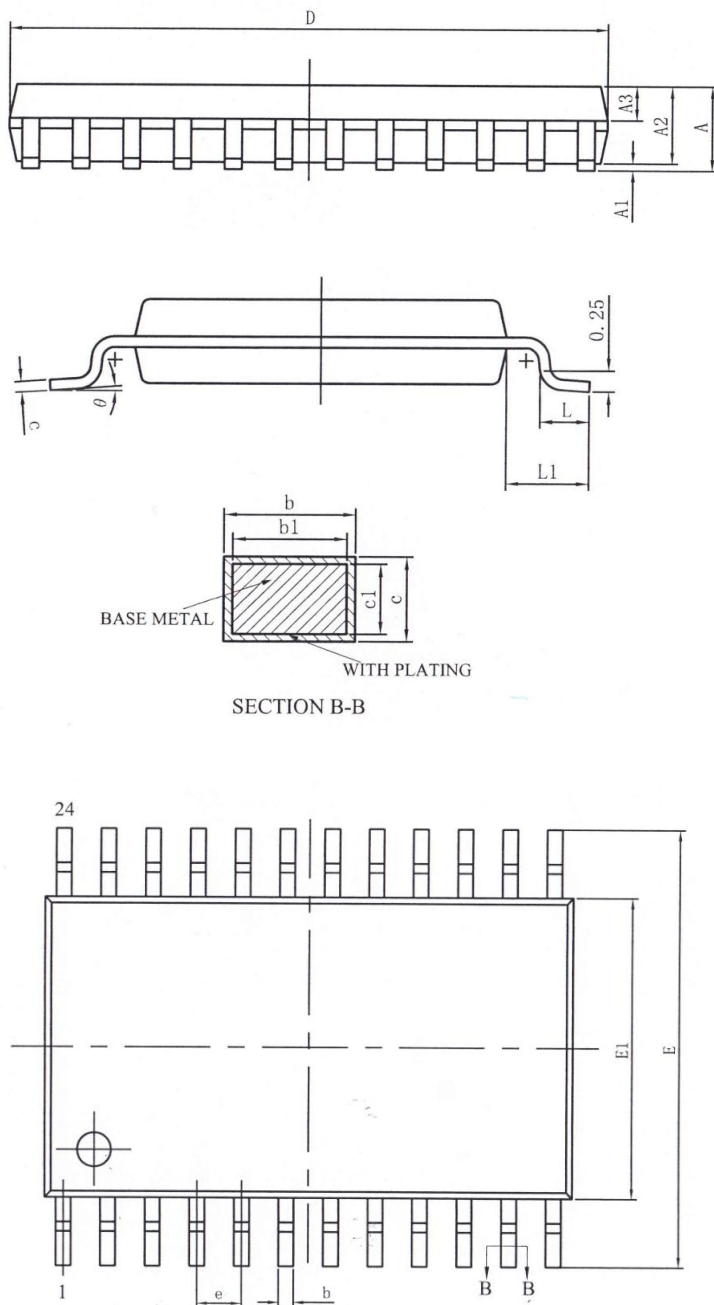


## 串口





## 5 Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
$\theta$	0	—	8°

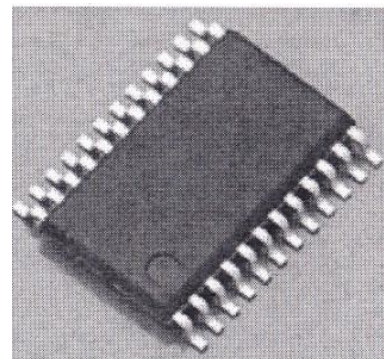


Figure 5- 1 TSSOP24 package dimensions