TG7221BM/TG7221BM-T5JE0 Datasheet

DS-TG7221BM V1.0

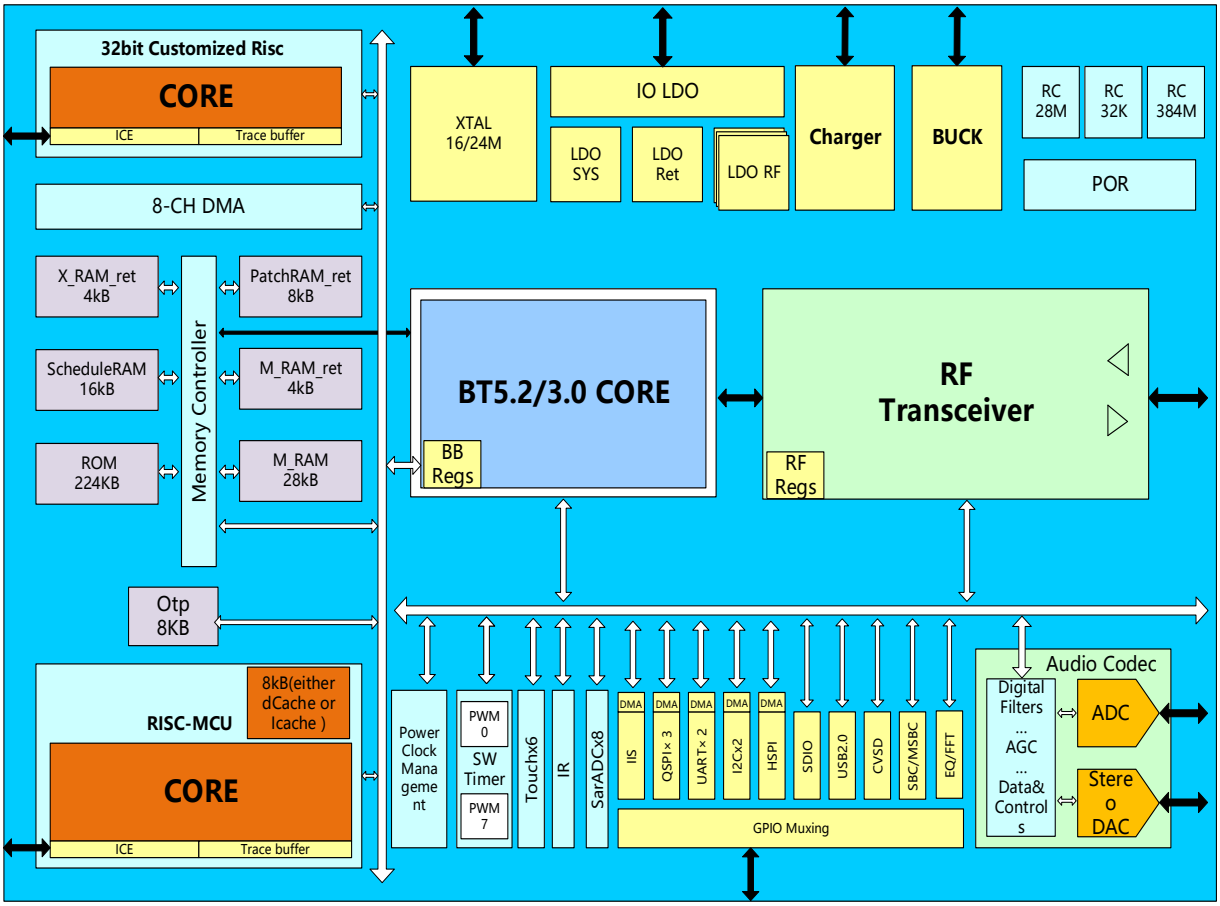
2024/1/31

目录

1. General Descriptions

TG7221BM-T5JE0 is a highly integrated SoC with Bluetooth 5.2 dual mode and high performance audio Codec. It also integrates 32 bit MCU and 192MHz Risc-V MCU to support various software features and product customization. TG7221BM-T5JE0 has been designed on highest level of integration to extremely reduce the number of external component. It is manufactured with advanced 40nm CMOS low leakage process which offers highest integration, lowest power consumption, lowest leakage current and reduced BOM cost.

错误!未找到引用源。 Block Diagram



2. Key Features

Bluetooth 5.2

- +10 dBm TX power @BLE
- +8 dBm TX power @EDR
- -97 dBm RX sensitivity @ BLE 1 Mbps
- -91.5 dBm RX sensitivity @ EDR 2 Mbps
- Fast AGC for enhanced dynamic range

Audio Codec

- Stereo 16/24-bit DAC，SNR 98dB
- Mono 16/-bit ADC，SNR 94dB
- Supports one PDM digital MIC inputs
- ADC Sampling rates of
  8KHz/11.025KHz/16KHz/22.05KHz/24KHz/
  32KHz/44.1KHz/48KHz are supported
- DAC Sampling rates of
  8KHz/11.025KHz/16KHz/22.05KHz/24KHz/
  32KHz/44.1KHz/48KHz/96KHz are supported
- Analog MIC amplifier, build-in MIC bias
  generator
- Two channels Stereo analog MUX
- Supports cap-less, single-ended, and
  differential mode at the DAC path
- Supports 16ohm and 32ohm Speaker loading

Dual CPU Architecture

- 32bit-RISC Core for link management
  - 120kB code ROM and 8KB otp
  - 20kB data RAM,including 4KB RAMs can be set to retention mode,
- RISC-V Core for application
  - 104KB ROM
  - Data RAM 40kB, including 4KB RAMs can be set to retention mode, 8kB （can be dcache or icache）

Up to 192MHz with float point unit

PMU

- Built-in LDO and DC-DC for the core, I/O, Bluetooth and flash
- Built-in charger for battery
- 3.7 uA current consumption in the soft-off mode

- VBAT is 1.65 V to 5.5V;

Audio Processing

- SBC, AAC , Audio decodes supported for BT audio
- mSBC voice codec supported for BT voice
- Supports MP3, WMA, FLAC, AAC, WAV, audio decoding
- Packet Loss Concealment (PLC) for voice processing
- Acoustic echo cancellation/suppression (AEC,AES)
- Single MIC Environmental Noise Cancellation (ENC)

Peripherals

- Up to 24 GPIOs with functions fully multiplexed
- 8-channel 12-bit ADC
- Built-in Low power Touch Key *6
- Built-in IR circuit
- Built-in T-scan （8 IO）
- Two-wire Master (I2C compatible), up to 600kbps;
- Two UART(RTS/CTS) with HCI-H5 protocol,
- SPI Master support
- Support Three QSPI and 1 HSPI
- 8x PWM support
- USB2.0 full speed, support host/slave mode
- SD Card Host Controller support
- I2S master/slave support
- 1 TRNG

Package

- TSSOP16 Package，5 x 6.4 mm, PN：TG7221BM
- TSSOP24 Package，7.8 x 6.4 mm ,PN：TG7221BM-T5JE0

3. Pinout Information

3.1 TG7221BM-T5JE0 Pinout information

Figure 3-1 TSSOP24 Pinout Top View

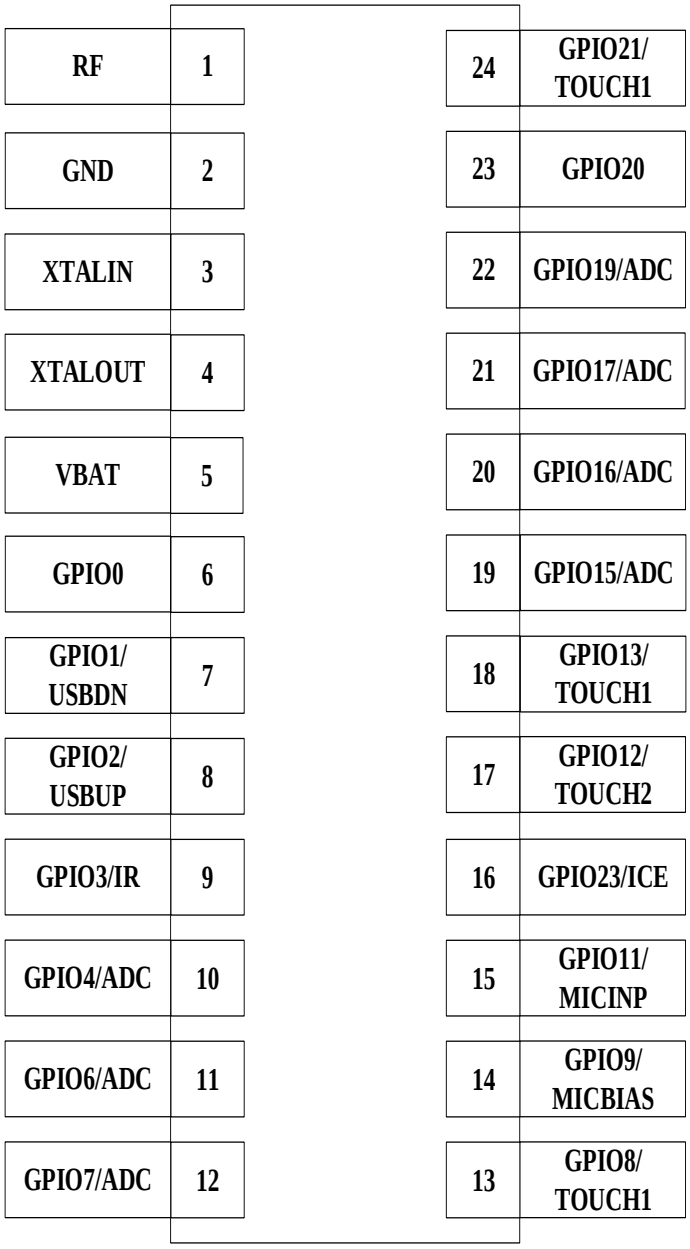


Table 3-1 Pinout Information of TSSOP24

TSSOP24	Pin Name	Type	Function Description
1	RF	RF_Port	ANT port
2	GND	GND	GND port
3	XTALIN	Ana_I	24M Crystal oscillator input
4	XTALOUT	Ana _O	24M Crystal oscillator output
5	VBAT	Power_I	Battery input
6	GPIO0	Dig _IO	pls check "sheet: GPIO_Muxing" ;
7	GPIO1/USBDN	Dig _IO	pls check "sheet: GPIO_Muxing" ; USB port.
8	GPIO2/USBDP	Dig _IO	pls check "sheet: GPIO_Muxing" ; USB port
9	GPIO3/IR	Dig _IO/Ana	pls check "sheet: GPIO_Muxing" ; Nec in IR out
10	GPIO4/ADC	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Measure Sar ADC
11	GPIO6/ADC	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Measure Sar ADC
12	GPIO7/ADC	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Measure Sar ADC
13	GPIO8/TOUCH1	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Touch pad 1
14	GPIO9/MICBIAS	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Power output for mic
15	GPIO11/MICNP	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Power input for mic
16	GPIO23/ICE	Dig _IO	pls check "sheet: GPIO_Muxing"
17	GPIO12/TOUCH2	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Touch pad 1
18	GPIO13/TOUCH1	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Touch pad 2
19	GPIO15/ADC	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Measure Sar ADC
20	GPIO16/ADC	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Measure Sar ADC
21	GPIO17/ADC	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Measure Sar ADC
22	GPIO19/ADC	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Measure Sar ADC
23	GPIO20	Dig _IO	pls check "sheet: GPIO_Muxing" ;

24	GPIO21/TOUCH1	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Touch pad 2

Table 3-2 GPIO Multiplexing

Pin Name	boot function	function-analog
GPIO[0]		
GPIO[1]	USBDN	
GPIO[2]	USBDP	
GPIO[3]	ir rx	
GPIO[4]		adc_channel0
GPIO[5]		adc_channel1
GPIO[6]		adc_channel2
GPIO[7]		adc_channel3
GPIO[8]	touch1c	
GPIO[9]	mic_bias	
GPIO[10]	min_inn	
GPIO[11]	mic_inp	
GPIO[12]	touch2c	linein_r
GPIO[13]	touch1b	linein_l
GPIO[14]	touch2b	
GPIO[15]		adc_channel4
GPIO[16]		adc_channel5
GPIO[17]		adc_channel6
GPIO[18]		
GPIO[19]		adc_channel7
GPIO[20]		xtal32k_in

GPIO[21]	touch1a	xtal32k_out
GPIO[22]	touch2a	
GPIO[23]	ICE	

3.2 TG7221BM Pinout information

Figure 3-2 TSSOP16 Pinout Top View

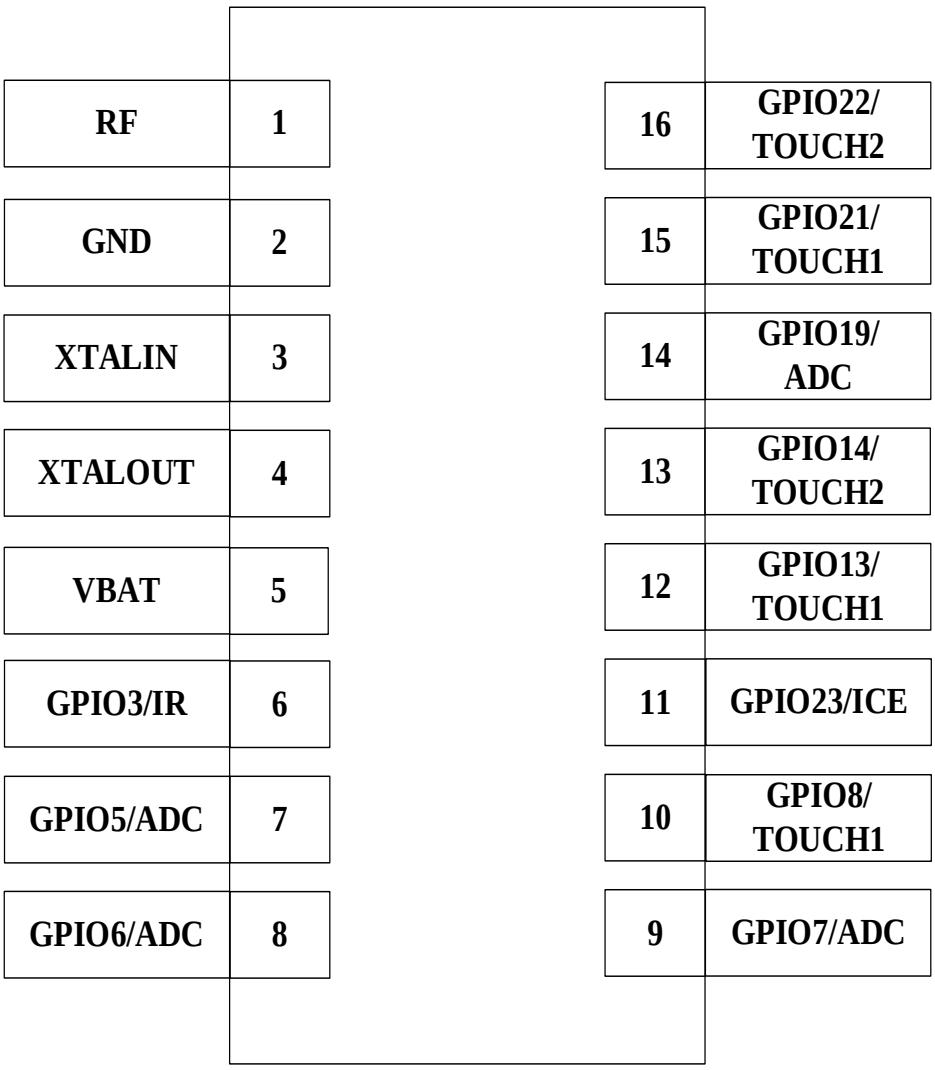


Table 3-3 Pinout Information of TSSOP16

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6	GPIO3/IR	Dig _IO/Ana	pls check "sheet: GPIO_Muxing" ; Nec in IR out
7	GPIO5/ADC	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Measure Sar ADC
8	GPIO6/ADC	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Measure Sar ADC
9	GPIO7/ADC	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Measure Sar ADC
10	GPIO8/TOUCH1	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Touch pad 1
11	GPIO23/ICE	Dig _IO/Dig _IO	pls check "sheet: GPIO_Muxing"
12	GPIO13/TOUCH1	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Touch pad 1
13	GPIO14/TOUCH2	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Touch pad 2
14	GPIO19/ADC	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Measure Sar ADC
15	GPIO21/TOUCH1	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Touch pad 1
16	GPIO22/TOUCH2	Dig _IO/Ana_O	pls check "sheet: GPIO_Muxing" ; Touch pad 2

Table 3-4 GPIO Multiplexing

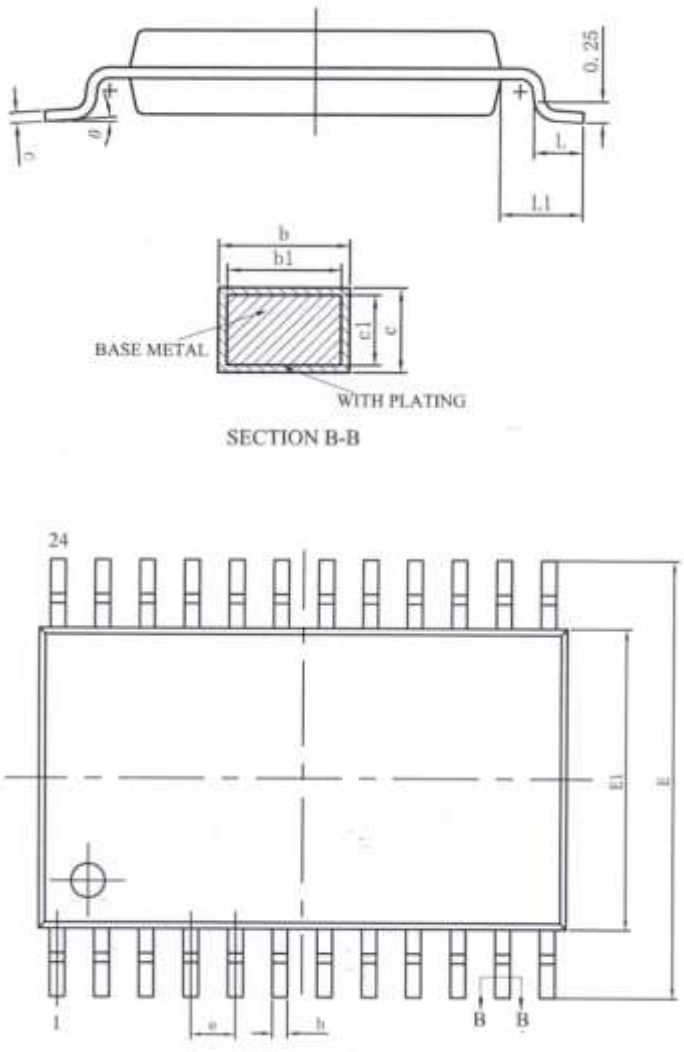
Pin Name	**boot function**	**function-analog**
GPIO[0]		
GPIO[1]	USBDN	
GPIO[2]	USBDP	
GPIO[3]	ir rx	
GPIO[4]		adc_channel0

GPIO[5]		adc_channel1
GPIO[6]		adc_channel2
GPIO[7]		adc_channel3
GPIO[8]	touch1c	
GPIO[9]	mic_bias	
GPIO[10]	min_inn	
GPIO[11]	mic_inp	
GPIO[12]	touch2c	linein_r
GPIO[13]	touch1b	linein_l
GPIO[14]	touch2b	
GPIO[15]		adc_channel4
GPIO[16]		adc_channel5
GPIO[17]		adc_channel6
GPIO[18]		
GPIO[19]		adc_channel7
GPIO[20]		xtal32k_in
GPIO[21]	touch1a	xtal32k_out
GPIO[22]	touch2a	
GPIO[23]	ICE	

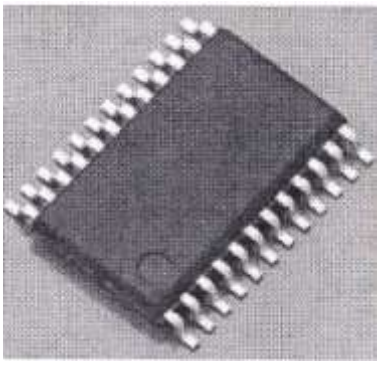
4. Package Information

4.1 TSSOP24 Package Information

Figure 4-1 TSSOP24 Package

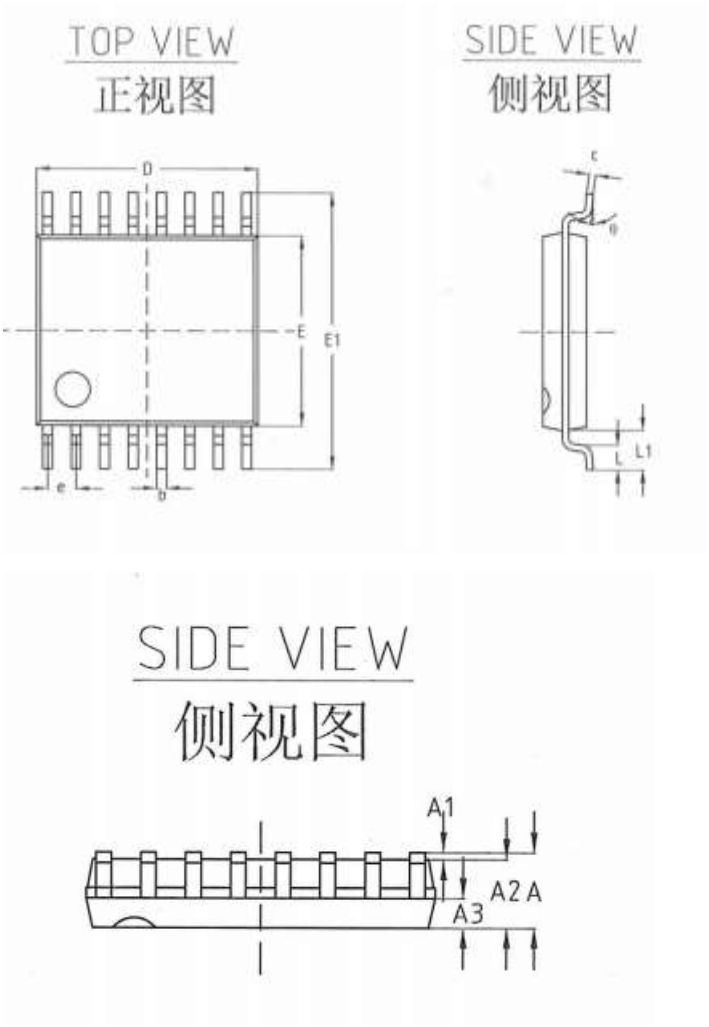


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0. 80	1. 00	1. 05
A3	0. 39	0. 44	0. 49
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0. 45	0. 60	0. 75
L1	1.00BSC		
θ	0	—	8°



4.2 TSSOP16 Package Information

Figure 4-2 TSSOP16 Package



机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
c	0.13	-	0.17
D	4.90	5.00	5.10
E	4.30	4.40	4.50
E1	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00REF		
L	0.45	0.60	0.75
θ	0°	-	8°

5. Specifications

5.1 Recommended Operating Conditions

Table 5-1 Recommended Operation Condition

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage for pin VBAT	V_{BAT}	Vth option with GND is 1.65V, otherwise 2.2V	1.65/2.2	3.3	5.5	V
Supply voltage for pin VDCDC	V_{DCDC}	Without BUCK ,	1.3	3.3	5.5	V
Charge voltage	V_{Charge}		4.5	5	5.5	V
Charge Current	I_{Charge}		20	40	140	mA
Trickle Charge Current	$I_{Trickle}$		2	16	56	mA
Ambient temperature	T_A		-40		85	° C

5.2 Power Consumption

Table 5-2 Power Consumption Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sleep						
Current through pin VBAT	I_{VBAT_SLEEP}	V_{BAT} = 3.3V		3.7		μA
RX mode 1 Mbps BLE @ -97 dBm sensitivity						
Current through pin VBAT	I_{VBAT_RX}	V_{BAT} = 3.3V	2.0	2.3	2.6	mA
Current through pin VDCDC	I_{VDCDC_RX}	V_{LDO} = 1.8V		10		mA
TX mode 0 dBm						
Current through pin VBAT	I_{VBAT_TX}	V_{BAT} = 3.3V		6.7		mA
Current through pin VDCDC	I_{VDCDC_TX}	V_{LDO} = 1.8V		18		mA

5.3 RF Radio

All parameters are referred to chip port and measured on the condition of VBAT = VIN = 3.3V if not stated otherwise.

Table 5-3 Transmitter Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	f_{TX}		2400		2483.5	MHz
Output power	P_{out}		-20.0	0	10	dBm
2nd harmonic power	P_{2harm}	0 dBm with external π type matching network		-43.0		dBm
3rd harmonic power	P_{3harm}	0 dBm with external π type matching network		-48		dBm
Spurious emissions (@ 0 dBm)	P_{spur}	30 MHz to 1000 MHz		-43.7		dBm
		1 GHz to 12.75 GHz		-40		dBm
		47 MHz to 74 MHz		-75		dBm
		87.5 MHz to 108 MHz		-75		dBm
		174 MHz to 230 MHz		-75		dBm
		470 MHz to 862 MHz		-44.0		dBm
BDR DH1						
Average frequency deviation	$\Delta f1_{avg\_BR}$	0 dBm	150	158	162	KHz
Average frequency deviation ratio	$\Delta f2_{avg\_BR}/\Delta f1_{avg\_BR}$	0 dBm	0.8	0.88	0.9	
Adjacent channel power (2MHz offset)	P_{adj_BR}	0 dBm	-55	-46	-50	dBm
Alternate adjacent channel power (3MHz offset)	P_{aadj_BR}	0 dBm	-58	-55	-53	dBm
EDR 2DH5						
PRF	RF output power		-20	0	8	dBm
PRF1	Adjacent channel power (2MHz offset)@0dBm			-34		dBm
PRF2	Adjacent channel power (3MHz offset)@0dBm			-37		dBm
Modulation Accuracy, EVM	RMS DEVM (π/4 DQPSK) @0dBm			7		%
	Peak DEVM (π/4 DQPSK) @0dBm			15		%

1 Mbps BLE						
Average frequency deviation	$\Delta f1_{avg, 1M}$	0 dBm		250		KHz
Average frequency deviation ratio	$\Delta f2_{avg\_1M}$/ $\Delta f1_{avg\_1M}$	0 dBm		0.87		
Adjacent channel power (2 MHz offset)	P_{adj_1M}	0 dBm		-48.4		dBm
Alternate adjacent channel power (3 MHz offset)	P_{aadj_1M}	0 dBm		-52.3		dBm
2 Mbps BLE						
Average frequency deviation	$\Delta f1_{avg\_2M}$	0 dBm		500		KHz
Average frequency deviation ratio	$\Delta f2_{avg\_2M}$/ $\Delta f1_{avg\_2M}$	0 dBm		0.8		
Adjacent channel power (4 MHz offset)	P_{adj_2M}	0 dBm		-56		dBm
Alternate adjacent channel power (6 MHz offset)	P_{aadj_2M}	0 dBm		-59		dBm

Table 5-4 Receiver Specification

Parameter	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Frequency range	f_{RX}		2400		2483.5	MHz
Out-of-band blocking	OOB	30 MHz – 2000 MHz	-30	-25	-20	dBm
		2003 – 2399 MHz	-35	-30	-25	dBm
		2484 – 2997 MHz	-35	-30	-25	dBm
		3000 MHz – 12.75 GHz	-30	-23	-25	dBm
Basic Rate						
RX sensitivity	P_{SENS_BR}	0.1 % BER	-95	-94		dBm
C/I co-channel	C/I_{CO_BR}	0.1 % BER		7	11	dB
C/I 1 MHz adjacent channel	C/I_{1_1M}	0.1 % BER		-9	0	dB
C/I 2 MHz adjacent channel	C/I_{2_1M}	0.1 % BER		-38.1	-30	dB
C/I ⩾3 MHz adjacent channel	C/I_{3_1M}	0.1 % BER		-44.9	-40	dB
C/I image channel	C/I_{im_1M}	0.1 % BER			-9	dB
C/I image channel + 1MHz	C/I_{im+1_1M}	0.1 % BER			-20	dB
Maximum input signal level	$P_{IN\_MAX\_1M}$	0.1 % BER		0.0	-20	dBm

EDR 2DH5						
RX sensitivity	P_{SENS_BR}	0.01 % BER	-94	-93	-91	dBm
C/I co-channel	C/I_{CO_BR}	0.01 % BER		9	13	dB
C/I 1 MHz adjacent channel	C/I_{1_1M}	0.01 % BER		-9	0	dB
C/I 2 MHz adjacent channel	C/I_{2_1M}	0.01 % BER		-40	-30	dB
C/I ⩾3 MHz adjacent channel	C/I_{3_1M}	0.01 % BER		-42	-40	dB
C/I image channel	C/I_{im_1M}	0.01 % BER		-27	-7	dB
C/I image channel + 1MHz	C/I_{im+1_1M}	0.01 % BER		-41	-20	dB
Maximum input signal level	$P_{IN\_MAX\_1M}$	0.01 % BER		-5	-20	dBm
1 Mbps BLE						
RX sensitivity	P_{SENS_1M}	30.8 % PER	-97.5	-97	-96	dBm
C/I co-channel	C/I_{CO_1M}	30.8 % PER		3.8	21	dB
C/I 1 MHz adjacent channel	C/I_{1_1M}	30.8 % PER		-9		dB
C/I 2 MHz adjacent channel	C/I_{2_1M}	30.8 % PER		-40.5	-17	dB
C/I ⩾3 MHz adjacent channel	C/I_{3_1M}	30.8 % PER		-46	-27	dB
C/I image channel	C/I_{im_1M}	30.8 % PER			-9	dB
C/I image channel + 1MHz	C/I_{im+1_1M}	30.8 % PER			-15	dB
Maximum input signal level	$P_{IN\_MAX\_1M}$	30.8 % PER		0.0	-10	dBm
2 Mbps BLE						
RX sensitivity	P_{SENS_2M}	30.8 % PER	-96	-94	-93	dBm
C/I co-channel	C/I_{CO_2M}	30.8 % PER		6	21	dB
C/I 2 MHz adjacent channel	C/I_{2_2M}	30.8 % PER		-11	15	dB
C/I 4 MHz adjacent channel	C/I_{4_2M}	30.8 % PER		-41	-17	dB
C/I ⩾6 MHz adjacent channel	C/I_{6_2M}	30.8 % PER		-45	-27	dB
C/I image channel	C/I_{im_2M}	30.8 % PER			-9	dB
C/I image channel + 2MHz	C/I_{im+2_2M}	30.8 % PER			-15	dB
Maximum input signal level	$P_{IN\_MAX\_1M}$	30.8 % PER		0.0	-10	dBm

5.4 24 MHz Crystal Oscillator

Table 5-5 24 MHz Crystal Oscillator Characteristic

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency	f_{XTAL}		16	24	32	MHz
Crystal frequency tolerance	Δf_{XTAL}		-20		20	ppm
Load capacitance	$C_{L,\ INN}$	Programmable via registers		12	20	pF

5.5 LDO Characteristics

Table 5-6 LDO Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage range	V_{IN}				5.5	MHz
Output voltage	V_{OUT_SLEEP}	I_{LOAD}=20 mA, when input voltage below 3.3V, output equals input		3.35		V
	V_{OUT_ACTIVE}	I_{LOAD}=100 μA, when input voltage below 3.3V, output equals input		3.35		V
Maximum load current	I_{LOAD}	Active mode，4.2V input		150		mA
Output load capacitance	C_L		0	1	4.7	μF
Quiescent current	I_{Q_SLEEP}	doze mode		50		nA
	I_{Q_ACTIVE}	active mode		50		μA

5.6 Reset Characteristics

Reset voltage is monitored on pin VBAT_HIGH.

Table 5-7 Reset Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset voltage threshold	V_{POR}	rising edge	1.65			V

			Or 2.2V			
POR stretch time	T_{POR}			30		mS
PDR stretch time	T_{PDR}			20		μS

5.7 DAC Characteristics

Table 5-8 Audio DAC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution		16	24	24	Bits
Full Scale Output Signal Level			1.1		Vrms
Sampling frequency		8		96	kHz
Dynamic Range	A- Weighted , 1kHz, -60dBFS input signal		101		dB
Signal to Noise Ratio	A- Weighted , 1kHz, 0dBFS, input signal		100		dB
Total Harmonic Distortion + Noise	Weighted ,1kHz, -6dBFS, input signal		-89		dB
Channel Separation			110		dB

5.8 ADC Characteristics

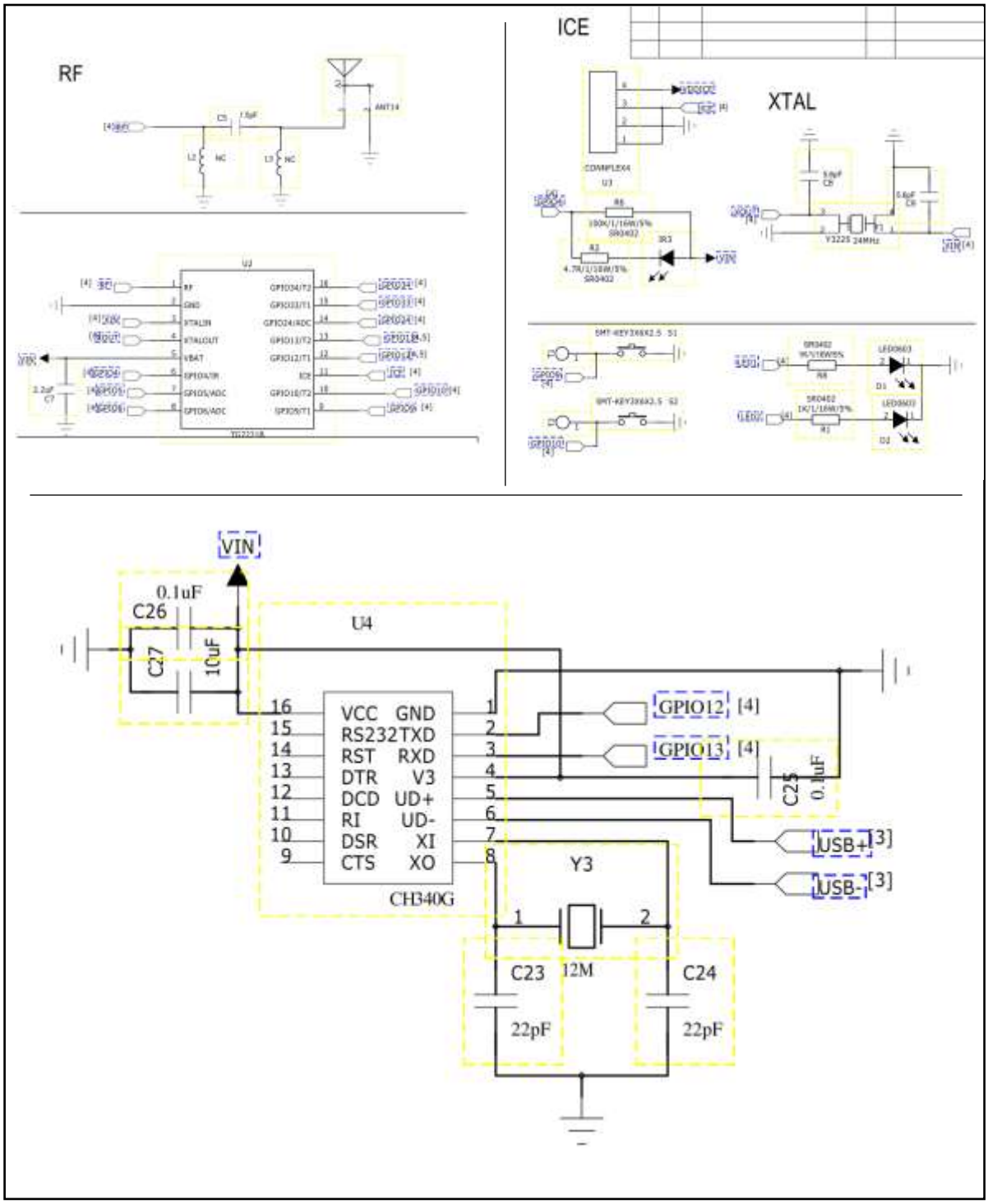
Table 5-9 Audio ADC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			16		Bits
Full Scale input Signal Level	Mic gain=0		1.1		Vrms
Sampling frequency		8		48	kHz

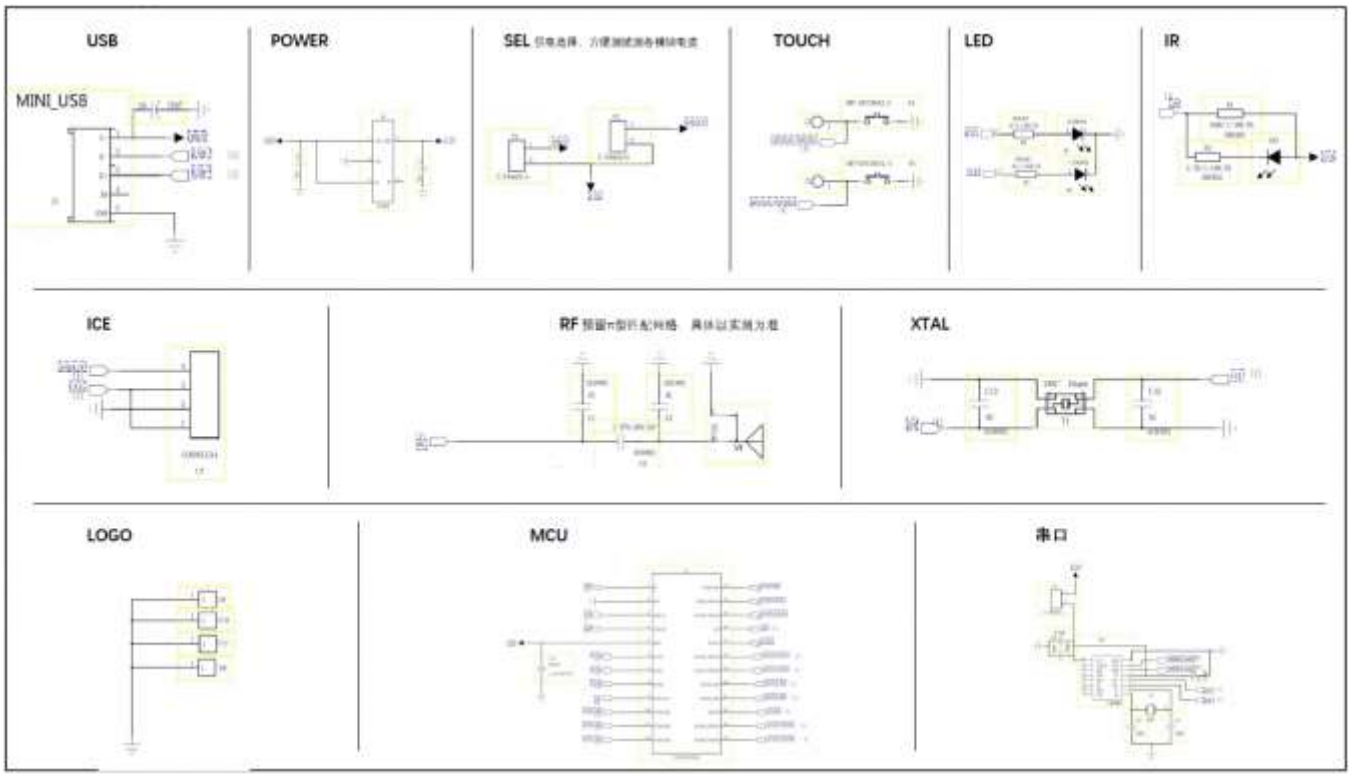
PGA Gain Range	1.5dB/step	0		46.5	dB
Input Resistance		20			kΩ
Dynamic Range	A-Weighted 1kHz input signal		93		dB
Signal to Noise Ratio	A-Weighted, 1kHz input signal		94		dB
Total Harmonic Distortion + Noise	Mic gain=0, Generator Level=2vrms,-1.2dbfs,1kHz input signal		-80		dB

6. Application Schematic

6.1 TSSOP16 Reference Design



6.2 TSSOP24 Reference Design



History

版本	日期	发布说明
1.0	2024/02/21	Initial release